GW3887A

Wireless LAN Integrated Medium Access Controller with Baseband Processor

The Conexant GW3887A Wireless LAN Integrated Media Access Controller with Baseband Processor is part of both the PRISM GT™ single band and PRISM WWR™ dual band radio chip sets. The GW3887A directly interfaces with Conexant's ISL3686B Single Band Direct Conversion Transceiver. Adding Conexant's ISL3084 5GHz VCO and ISL3980 Power Amp completes an end-to-end WLAN chip set solution compliant with 802.11b/g standards. Additionally, the GW3887A directly interfaces with Conexant's ISL3692 Dual Band Direct Conversion Transceiver. Adding Conexant's ISL3092 11GHz VCO and ISL3992 Dual Band Power Amp completes an end-to-end WLAN chip set solution compliant with 802.11a/b/g/h/i/j standards. The 802.11 protocol is implemented in firmware supporting custom WLAN solutions.

The GW3887A improvements over the GW3887 include the addition of an internal 48MHz oscillator, which eliminates several external components from the radio design.

Software implements the full IEEE 802.11 Wireless LAN MAC protocol. It supports BSS and IBSS operation under DCF, and operation under the optional Point Coordination Function (PCF). Active scanning is performed autonomously once initiated by host command. Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers.

Orthogonal Frequency Division Multiplexing (OFDM) of 52 sub-carriers modulated with BPSK, QPSK, 16QAM or 64QAM and a variety of convolutional coding rates provides 8 selectable data rates at 2.4GHz and 5GHz. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability along with Complementary Code Keying provide an additional 4 selectable data rates at 2.4GHz.

Built-in flexibility allows the GW3887A to be configured for a range of applications. The MAC is based on the ARM 946E processor core that offers a wide variety of code development support tools.

The GW3887A is housed in a thin plastic BGA package suitable for USB 2.0 Wireless LAN small form factor circuit card applications.

Features

- Firmware implements the full IEEE 802.11a/b/g/h/i/j Wireless LAN MAC protocols
- Internal WEP Engine allows 64 or 128 bit Encryption
- AES Hardware Accelerator
- Start-up modes allow the USB vendor and device ID to be initialized from a small external serial EEPROM. This allows firmware to be downloaded from the host.
- On-chip SRAM memory
- A low frequency crystal oscillator can maintain time, which allows the high frequency clock source to be powered off during sleep mode.
- Firmware controlled antenna diversity
- Data Rates: 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, & 54Mbps
- Modulation: OFDM with BPSK, QPSK, 16QAM, 64QAM; DBPSK; DQPSK and CCK
- Convolutional coding and interleaving on all OFDM rates
- Targeted for OFDM Multipath Delay Spreads >800ns for 6Mbps, and >100ns for 54Mbps
- Targeted for CCK Multipath Delay Spreads >90ns at 11Mbps, >200ns at 5.5Mbps and >360ns at 1 and 2Mbps
- Direct interface with the ISL3692 and ISL3686 Direct Conversion transceiver
- USB 2.0 Wireless LAN Adapters

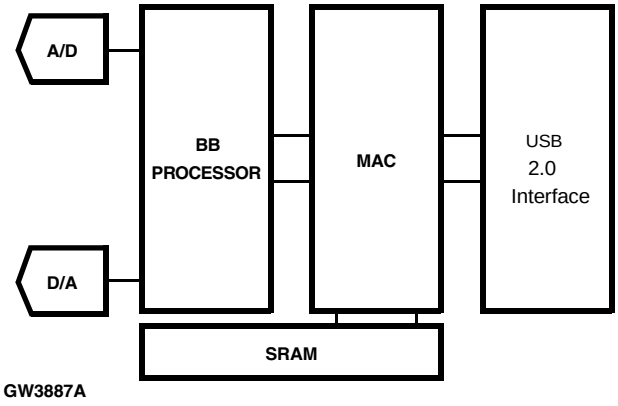


Figure 1: Simplified Block Diagram

1 Signal Descriptions

Table 1 provides detailed pin information.

Table 1: GW3887A Signal Descriptions (Sheet 1 of 5)

Pin Name	BGA Ball Assignment	Pad Type	Pin I/O TYPE	Description
coreVDDD	a1	supply	none	Digital core supply(1.8V)
coreVDDD	a10	supply	none	Digital core supply(1.8V)
ioVDDD	a11	supply	none	Digital IO supply (3.3V)
GNDD	a12	supply	none	Digital IO and core ground
coreVDDD	a13	supply	none	Digital core supply(1.8V)
ioVDDD	a14	supply	none	Digital IO supply (3.3V)
TEST1	a15	Bidir as output	none	BBP testbus
TEST6	a16	Bidir as output	none	BBP testbus
SERCLK	a2	Input		Serial Host Clock
SERDIN	a3	BIDIR		Serial host data in for 4-wire interface. Bidir for 3 wire interface
coreVDDD	a4	supply	none	Digital core supply(1.8V)
ioVDDD	a5	supply	none	Digital IO supply (3.3V)
TDI	a6	Bidir as input	up	JTAG test serial data input
coreVDDD	a7	supply	none	Digital core supply(1.8V)
ioVDDD	a8	supply	none	Digital IO supply (3.3V)
TMSEL2	a9	Bidir as input	down	Testmode select pin
GP2-13	b1	bidir	up	General purpose
UTMI-2	b10	Input	none	UTMI_LineState[1]
UTMI-1	b11	Input	none	UTMI_LineState[0]
TEST4	b12	Bidir as output	none	BBP testbus
GNDD	b13	supply	none	Digital IO and core ground
TSTCLK44in	b14	Schmitt input	down	ATE 44MHz clock in
TSTCLK80in	b15	Schmitt input	down	ATE 80MHz clock in
coreVDDD	b16	supply	none	Digital core supply(1.8V)
ioVDDD	b2	supply	none	Digital IO supply (3.3V)
GNDD	b3	supply	none	Digital IO and core ground
UartSIN	b4	Schmitt input	down	Uart serial data input
GNDD	b5	supply	none	Digital IO and core ground
TMS	b6	Bidir as input	up	JTAG test mode select
TDO	b7	bidir	none	JTAG test serial data output
TMSEL1	b8	Bidir as input	down	Testmode select pin
coreVDDD	b9	supply	none	Digital core supply(1.8V)
GP2-11	c1	bidir	up	CSTSCHG
TEST10	c10	Bidir as output	none	BBP testbus
TEST9	c11	Bidir as output	none	BBP testbus
TEST3	c12	Bidir as output	none	BBP testbus
TEST2	c13	Bidir as output	none	BBP testbus
TEST0	c14	Bidir as output	none	BBP testbus (LSB)
IoVDDD	c15	supply	none	Digital IO supply (3.3V)
CLKOUT	c16	Bidir as output	none	40MHz clock out
UartSOUT	c2	Bidir as output	none	Uart output pad
SERCS_N	c3	Input		Serial Host Chip Select
SERINT	c4	Output		Serial Host Interrupt

Table 1: GW3887A Signal Descriptions (Sheet 2 of 5)

Pin Name	BGA Ball Assignment	Pad Type	Pin I/O TYPE	Description
RESETn	c5	Schmitt input	up	Active low reset for chip
GNDD	c6	supply	none	Digital IO and core ground
TMSEL3	c7	Bidir as input	down	Testmode select pin
TMSEL0	c8	Bidir as input	down	Testmode select pin
GNDD	c9	supply	none	Digital IO and core ground
IoVDDD	d1	supply	none	Digital IO supply (3.3V)
TEST7	d10	Bidir as output	none	BBP testbus
TEST5	d11	Bidir as output	none	BBP testbus
coreVDDD	d12	supply	none	Digital core supply(1.8V)
UTMI-0	d13	input	none	UTMI_CLK
OSCENABLE	d14	Bidir as output	none	Canned oscillator enable signal, high is active
GNDD	d15	supply	none	Digital IO and core ground
coreVDDD	d16	supply	none	Digital core supply(1.8V)
GP2-12	d2	bidir	up	Multi-ICE RTCK
GP2-9	d3	Bidir	up	LED1 Activity LED (and Uart BaudOut_N)
SERDOUT	d4	Output	none	Serial host data out for 4-wire interface
UTMI-3	d5	Output	none	UTMI_TxValid
TRSTn	d6	Bidir as input	up	JTAG test reset
TCK	d7	Bidir as input	up	JTAG test clock
TEST11	d8	Bidir as output	none	BBP testbus (MSB)
TEST8	d9	Bidir as output	none	BBP testbus
coreVDDD	e1	supply	none	Digital core supply(1.8V)
GNDD	e13	supply	none	Digital IO and core ground
ioVDDD	e14	supply	none	Digital IO supply (3.3V)
LNA_H/L	e15	Bidir as output	none	AGC 30dB pad signal
CLKIN40	e16	Schmitt input	none	High frequency (40MHz) crystal pad cell
GP1-3	e2	bidir	down	PA_PE5G 5GHz PA enable
GP1-2	e3	bidir	down	USB_VBUS
FAA_HRDn	e4	Schmitt	up	Hardware input for FAA switch
ioVDDD	f1	supply	none	Digital IO supply (3.3V)
ANALOG_TEST	f13	Input/Output	-	Voltage used in conjuction with ATE testing
VSSA33C	f14	supply	-	USB2.0 Common Analog ground
VSSDPHY	f15	supply	none	Gnd for Digital portion of USB Phy
VDDDPHY	f16	supply	none	1.8V supply for Digital portion of USB Phy
GP2-4	f2	bidir	down	Uart DTR_N
GP2-7	f3	bidir	down	Uart CTS_N
GP1-15	f4	bidir	up	FAAmode_n
coreVDDD	g1	supply	none	Digital core supply(1.8V)
NC	g13	none	none	No connect, no pad
VDDA33C	g14	supply	-	USB2.0 Common Analog supply
XI	g15	analog	-	48-Mhz Crystal or clock input if external clock used
XO	g16	analog	-	48-Mhz Crystal output. Unused unless using external crystal
GP2-6	g2	bidir	down	Uart RTS_N
GP2-8	g3	bidir	up	Uart DCD_N
GNDD	g4	supply	none	Digital IO and core ground
GP2-2	h1	bidir	down	FAA LED (LED2)

Table 1: GW3887A Signal Descriptions (Sheet 3 of 5)

Pin Name	BGA Ball Assignment	Pad Type	Pin I/O TYPE	Description
NC	h13	none	none	No connect, no pad
VSSA33T	h14	supply	-	USB2.0 Transceiver ground
REXT	h15	Input	-	External resistor 3.01K ohm (1%)
VDDA33T	h16	supply	-	USB2.0 Transceiver Supply
GP1-13	h2	bidir	up	RADIO_PE
GNDD	h3	supply	none	Digital IO and core ground
GP2-5	h4	bidir	down	Uart DSR_N
ioVDDD	j1	supply	none	Digital IO supply (3.3V)
VSSA33T	j13	supply	-	USB2.0 Transceiver ground
NC	j14	none	none	No connect, no pad
VSSA33T	j15	supply	-	USB2.0 Transceiver ground
DM	j16	analog	-	USB2.0 Data M Signal
coreVDDD	j2	supply	none	Digital core supply(1.8V)
GP2-1	j3	bidir	float	Serial flash data (SerDat)
GP2-3	j4	bidir	down	General purpose
GP1-14	k1	bidir	up	ANTSEL
COMPpabias	k13	analog	none	Compensation cap for PA bias DAC
PAbias5G	k14	analog	none	PAbiasSel5G = 1 For bias control of the 5GHz PA using a 6bit DAC
VDDA33T	k15	supply	-	USB2.0 Transceiver Supply
DP	k16	analog	-	USB2.0 Data P Signal
GP1-8	k2	bidir	down	PE2
GNDD	k3	supply	none	Digital IO and core ground
GP2-0	k4	bidir	down	Serial flash clock (SerCLK)
GP1-11	l1	bidir	down	ANTSEL
LOOP48	l13	analog	none	Loop compensation network for 48Mhz output PLL
VDDA6	l14	analog	none	Analog supply for PA bias DAC
GNDA6	l15	analog	none	Analog ground for PA bias
NC	l16	none	none	No connect, no pad
GP1-5	l2	bidir	down	SYNTHCLK
GP2-10	l3	bidir	up	Serial Flash Chip Select and RX/TX observe
GP1-12	l4	bidir	up	TRSW
ioVDDD	m1	supply	none	Digital IO supply (3.3V)
GNDAPLL	m13	analog	none	PLL ground
VDDAPLL	m14	analog	none	PLL supply voltage
VDDAPLL	m15	analog	none	PLL supply voltage
PAbias2G	m16	analog	none	PAbiasSel5G = 0 For bias control of the 2.4GHz PA using a 6bit DAC
GP1-7	m2	bidir	down	PA_PE2G 2.4Ghz PA enable.
GP1-0	m3	Bidir	down	PE1
GP1-9	m4	bidir	down	PLL_LD (PLL lock detect)
coreVDDD	n1	supply	none	Digital core supply(1.8V)
COMPiq	n10	analog	none	Compensation cpa for Tx DACs
RX_IF_det	n11	analog	none	Overload detector input
VDDA5	n12	analog	none	Analog supply for RX and TX AGC DACs
COMPtx	n13	analog	none	Compensation Cap for Tx AGC DAC
VDDAPLL	n14	analog	none	PLL supply voltage
LOOP80	n15	analog	none	Loop compensation network for 80Mhz output PLL

Table 1: GW3887A Signal Descriptions (Sheet 4 of 5)

Pin Name	BGA Ball Assignment	Pad Type	Pin I/O TYPE	Description
FSADpabias	n16	analog	none	Full scale adjust resistor for PA bias DAC
GP1-6	n2	Bidir	down	SYNTHDAT
LFXTALOUT	n3	Xtal output	-------	Low frequency (32kHz) crystal pad
LFXTALIN	n4	Xtal input	--------	Low frequency (32kHz) crystal pad
GNDD	n5	supply	none	Digital IO and core ground
GNDA1	n6	analog	none	Analog ground to 12bit DACs
FSADoff	n7	analog	none	Full scale adjust resistor for 12bit DACS
VDDA3	n8	analog	none	Analog supply to ADCs
GNDA3	n9	analog	none	Analog ground to ADCs
GNDD	p1	supply	none	Digital IO and core ground
FSADiq	p10	analog	none	Full scale adjust resistor for Tx DACs
GNDA4	p11	analog	none	Analog ground for Tx DACs
RX_IFagc_N	p12	analog	none	Iout- for BB Rx AGC DAC (BB_AGC-)
FSADtx	p13	analog	none	Full scale adjust resistor for Tx AGC DAC
VSUB2	p14	analog	none	Substrate pad (ground)
LOOP44	p15	analog	none	Loop compensation network for 44MHz output PLL
GNDAPLL	p16	analog	none	PLL ground
GP1-4	p2	Bidir	down	SYNTH_LE
GP1-10	p3	Bidir	down	TRSW
VDDA1	p4	analog	none	Analog supply to offset DACs (2.85V)
VDDD0	p5	analog	none	Offset DACs digital supply (2.85V)
VDDA2	p6	analog	none	Analog supply to offset DACs
VREF	p7	analog	none	Band gap voltage reference input
Iref	p8	analog	none	Current reference resistor
VDDA4	p9	analog	none	Analog supply to Tx DACs
ioVDDD	r1	supply	none	Digital IO supply (3.3V)
Qout_P	r10	analog	none	Iout+ for Q Tx DAC (TXQ+)
TX_IQ_det	r11	analog	none	When CalModeEN=1 this is selected as input to TXDET ADC
COMPrx	r12	analog	none	Compensation cap for Rx AGC DAC
GNDA5	r13	analog	none	Analog ground for RX and TX AGC DAC
VDDD1	r14	analog	none	Digital supply for DACs other than offset (2.85V)
NC	r15	none	none	No connect, no pad
GNDAPLL	r16	analog	none	PLL ground
GP2-14	r2	Bidir	up	LED0
coreVDDD	r3	supply	none	Digital core supply(1.8V)
VSUB1	r4	analog	none	Substrate tie (ground)
NC	r5	none	none	No connect, no pad
COMPioff	r6	analog	none	Comp pin for offset DACs
Iin_N	r7	analog	none	Input signal for I Rx ADC (RXI-)
Qin_P	r8	analog	none	Input signal + for Q Rx ADC (RXQ+)
Iout_P	r9	analog	none	Iout+ for I Tx DAC (TXI+)
GP1-1	t1	Bidir	down	HB_LB (High band/ Low Band) high band when
Qout_N	t10	analog	none	Iout- for Q Tx DAC (TXQ-)
PA_det	t11	analog	none	When CalModeEN=0 this is select as input to TXDET ADC
RX_IFagc_P	t12	analog	none	Iout+ for BB Rx AGC DAC (BB_AGC+)
FSADrx	t13	analog	none	Full scale adjust resistor for Rx AGC DAC

Table 1: GW3887A Signal Descriptions (Sheet 5 of 5)

Pin Name	BGA Ball Assignment	Pad Type	Pin I/O TYPE	Description
TX_IFagc	t14	analog	none	Iout for Tx AGC DAC
GNDD1	t15	analog	none	Digital ground for DACs other than offset
NC	t16	none	none	No connect, no pad
GNDD0	t2	analog	none	Offset DACs digital ground
Qoout_P	t3	analog	none	Iout+ for Q offset DAC (QOFFSET+)
Qoout_N	t4	analog	none	Iout- for Q offset DAC (QOFFSET-)
Ioout_P	t5	analog	none	Iout+ for I offset DAC (IOFFSET+)
Ioout_N	t6	analog	none	Iout- for I offset DAC (IOFFSET-)
Iin_P	t7	analog	none	Input signal + for I Rx ADC (RXI+)
Qin_N	t8	analog	none	Input signal for Q Rx ADC (RXQ-)
Iout_N	t9	analog	none	Iout- for I Tx DAC (TXI-)

2 Thermal Information

Thermal resistance information is provided in Table 2.

Table 2: Thermal Resistance[a]

Product	θ_{JA} (°C/W)
BGA Package	42

a. θJA is measured with the component mounted on high effective thermal conductivity test board in free air. Refer to DO-406099-TC Technical Brief(TB379) - Thermal Characterization of Packaged Semiconductor Devices for details.

Maximum Storage Temperature Range . . . . . -65°C to 150°C

Maximum Junction Temperature . . . . . 125°C

NOTE:

For recommended soldering conditions refer to DO-405727-TC Technical Brief (TB334) - Guidelines for Soldering Surface Mount Components to PC Boards.

3 Electrical Specifications

The GW3887A has an ESD classification of Class 1C. Electrical specifications for the GW3887A are provided in Table 3.

WARNING:

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 3: Electrical Specifications[a] (Sheet 1 of 2)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Absolute Maximum Ratings						
Supply Voltage	V_{cc}	-		3.3	3.6	V
Supply Voltage	V_{cc}	-		2.85	3.3	V
Supply Voltage	VDD_Core	-		1.8	1.98	V
Input, Output or I/O Voltage		-	GND - 0.3		V_{cc} + 0.3	V
Operating Conditions						
Voltage	VDD_I/O	-	3.0	3.3	3.6	V
Voltage	VDDD	-	2.7	2.85	3.3	V
Voltage	VDDA_PLL	-	2.7	2.85	3.3	V
Voltage	VDDA	-	2.7	2.85	3.3	V
Voltage	VDD_Core	-	1.62	1.8	1.98	V
Ambient Temperature Range	-	-	-40		85	^{o}C
DC Electrical Specifications						
Power Supply Current (3.3V)	I_{CCOP}	V_{CC} = 3.6V, CLK Frequency 80MHz	-	-	10	mA
Power Supply Current 2.85V)	I_{CCAOP}	V = 3.3V, Rx	-	-	100	mA
Power Supply Current (1.8V)	I_{CORE}	V = 1.98V, Rx 54Mbps packet	-	-	300	mA
Standby Current (3.3V)	I_{CCstby}	VCC = 3.3V, Using 32kHz LF XTAL, T_A = 25°C	-	-	300	µA
Standby Current (2.85V)	I_{CCstby}	V = 2.85V, Using 32kHz LF XTAL, T_A = 25°C	-	-	150	µA
Standby (1.8V)	I_{CCstby}	V = 1.8V, Using 32kHz LF XTAL, T_A = 25°C	-	-	100	µA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-15	1	15	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-15	1	15	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max, Min (V_{CC}=VDD_I/O)	$0.7V_{CC}$	-	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min, Max (V_{CC}=VDD_I/O)	-	-	$0.3V_{CC}$	V
Logical One Output Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Min (V_{CC}=VDD_I/O)	$0.9V_{CC}$	-	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min (V_{CC}=VDD_I/O)	-	0.1	$0.1V_{CC}$	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz. All measurements referenced to GND. T_A = 25°C	-	5	10	pF
Output Capacitance	C_{OUT}	CLK Frequency 1MHz. All measurements referenced to GND. T_A = 25°C	-	5	10	pF
Schmitt Hysteresis	-		0.4	-	0.6	V

Table 3: Electrical Specifications[a] (Sheet 2 of 2)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
AC Electrical Specifications						
CLOCK SIGNAL TIMING						
OSC Clock Frequency (40MHz ±20ppm max, duty cycle 45/55)	t_{CYC}		-	40	-	MHz
SYNTHESIZER						
SYNTHCLK(GP1-5) Width Hi	t_{SCLKHI}		50	-	-	ns
SYNTHCLK(GP1-5) Width Hi	t_{SCLKLO}		50	-	-	ns
Synthesizer Data Setup Time (SYNDATA, GP1-6)	$t_{SYNSETUP}$		50	-	-	ns
Synthesizer Data Hold Time	$t_{SYNHOLD}$		10	-	-	ns
LE pulse width (LE_IF, GP1-1 and LE_RF GP1-2)	t_{LE}		50	-	-	ns

a. Controlled via design or process parameters and not directly tested.

4 MAC Overview

The GW3887A MAC uses an ARM946E-S core. The MAC is capable of operating at frequencies from 32kHz in a reduced functionality power save mode up to 80MHz in normal operation.

The GW3887A is equipped with on chip memory, which is used for instruction memory and data buffers. No external SRAM is required.

The GW3887A is designed for use with a USB 2.0 host interface in accordance with the USB 2.0 specification. The GW3887A is designed for device side applications. The TMSEL[3:0] signals are used to select special test modes and are unterminated for standard applications.

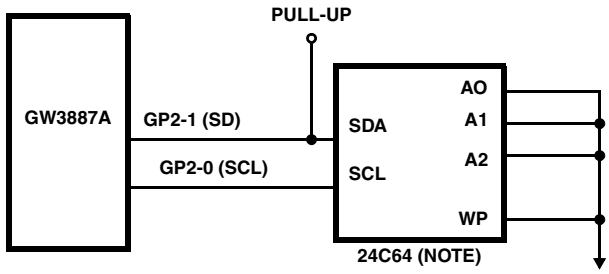
The GW3887A is equipped with 31 general purpose I/Os. These GPIOs are divided into two groups, GP1[15:0] and GP2[14:0]. In general, the GP1 I/Os are used for radio control functions while the GP2 can be used for additional features under firmware control.

5 Hardware WEP Engine

The Wired Equivalent Privacy Module (WEP) accelerates data encryption and decrypting providing a level of security for a wireless network that is intended to be at least as good as that of a wired network. The encryption protocol used is RSA RC4. For more information about the WEP RC4 encryption, see IEEE Std. 802.11 1994 section 8.2.

6 Serial EEPROM Interface

The GW3887A allows the USB vendor ID and product ID information and a small firmware image to be transferred from an off-chip serial non-volatile memory device to on-chip RAM after a system reset. This allows a system vendor specific configuration. The operating frequency of the serial port is 400kHz with a voltage of 3.3V.



NOTE: Must operate at 400kHz at 3.3V_{DC}.

Figure 2: Small Serial EEPROM Interface

7 Reset

Power-on reset must be asserted via the RESET# pin to the GW3887A until 10µs after establishing acceptable power supply levels and stable clock signals. The TMSEL[0.3] are sampled on the rising edge of RESET# to determine the boot mode. These pins have internal pull down resistors with an effective resistance of about 50K.

8 Baseband Processor Interface

The interface to the baseband processor is mostly internal, but some of the connections are visible on the GP2 and test ports when properly configured.

9 Radio Power Sequencing

The GW3887A provides a number of firmware controlled pins that are used for controlling the power sequencing components in the radio.

Packet transmission requires precise control of the radio. Ideally, energy at the antenna ceases after the last symbol of information has been transmitted. Since the GW3887A is designed for use with both 5GHz and 2.4GHz radios, it provides signals capable of controlling multiple power amplifiers or one dual band amplifier. Additionally, the transmit/receive switch must be controlled properly to protect the receiver. It's also important to apply appropriate modulation to the PA while it's active.

Signaling sequences for the beginning and end of normal transmissions are illustrated in Figure 3.

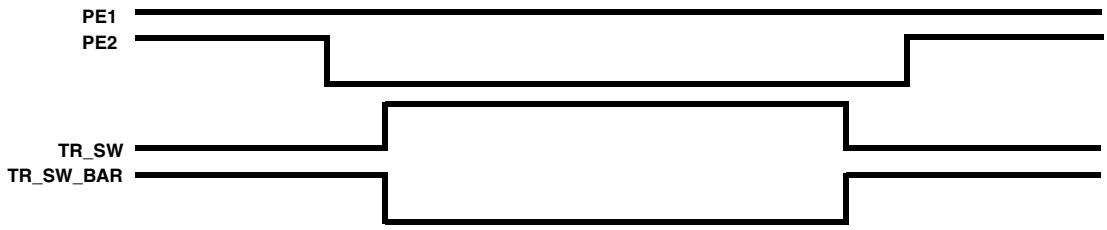


Figure 3: Transmit Control Signal Sequencing

A transmission begins with a transmit enable (TX_ENABLE) to the Baseband processor inside the GW3887A. This enable activates the transmit state machine in the BBP. Next, 2GPABIAS activates the PA for 802.11b or g transmission followed by PE2 being activated. Alternately 5GPABIAS can activate the PA for 802.11a transmission. Lastly, the transmit/receive switch is configured for transmission via the differential pair TR_SW and TR_SW_BAR. Delays for these signals related to the initiation of transmission are referenced to TX_ENABLE.

After the GW3887A sends the last data, it de-asserts the appropriate PABIAS signal, PE2, and TR_SW.

PE1 and PE2 encoding details are found in Table 4.

Note that during normal receive and transmit operation that PE1 is static and PE2 toggles for receive and transmit states.

Table 4: Power Enable States[a]

	PE1	PE2	PLL_PE
Power Down State	0	0	1
Receive State	1	1	1
Transmit State	1	0	1
PLL Active State	0	1	1
PLL Disable State	X	X	0

a. PLL_PE is controlled via the serial interface, and can be used to disable the internal synthesizer, the actual synthesizer control is an AND function of PLL_PE, and a result of the OR function of PE1 and PE2. PE1 and PE2 will directly control the power enable functionality of the LO buffer(s)/phase shifter.

10 Master Clock and Low-Frequency Crystal

The GW3887A MAC controller accepts the same clock signal as the PHY baseband processor (40MHz), thereby avoiding the need for a separate, MAC-specific oscillator. The GW3887A also has a low-frequency oscillator. This low-frequency oscillator is intended for use with a 32kHz, tuning-fork type watch crystal to permit accurate timekeeping with very low power consumption during sleep state.

A very low power sleep mode allows the GW3887A device to be clocked from an external crystal source, in place of the CLK input. An output, OSCENABLE, is deasserted to allow the external oscillator that generates CLKIN to be disabled to save power. When the clocks have switched, all internal clocks are generated from the crystal source.

To transition out of deep sleep, the OSCENABLE output is asserted to re-enable the external oscillator. Some time later (typically 10ms), the oscillator outputs are stable and the GW3887A device is switched back to the high frequency CLK source.

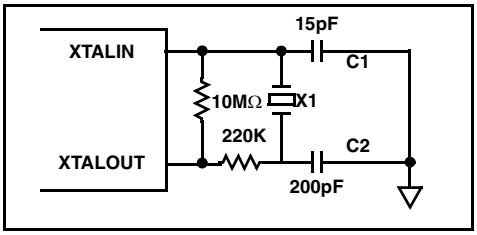


Figure 4: 32kHz Crystal

11 Power Up Sequencing

I/O structures may draw excessive current if the core voltage is not applied which, when prolonged and excessive, can reduce the usable life of the device. The safest way to power up the device is to sequence the core and I/O power. The core should be powered up prior to the I/O block. The I/O voltage should be applied after the core voltage has reached at least 90% of its regulated level. Bringing the core and I/O supplies to their respective regulation levels in a maximum time frame of 100ms moderates the stresses placed on both the power supply and the device. Sequencing is not required when powering down. However, all power must be removed within 100mS of the removal of any power supply.

From Figure 5, the sequence delay for turning on the I/O power supply (t_{io}-t_{pg}) should be no less than 0ms and no greater than 100ms.

12 Proper Handling

All integrated circuits are susceptible to damage by inappropriate handling. Damage is often caused by Electrostatic Discharge (ESD) or inappropriate moisture content when soldering. The GW3887A has a moisture sensitivity classification of level 2 for GW3887AIK and GW3887AIK-T5 and level 3 for GW3887AIKZ-T5 in accordance with IPC/JEDEC J-STD-020A and should be handled accordingly.

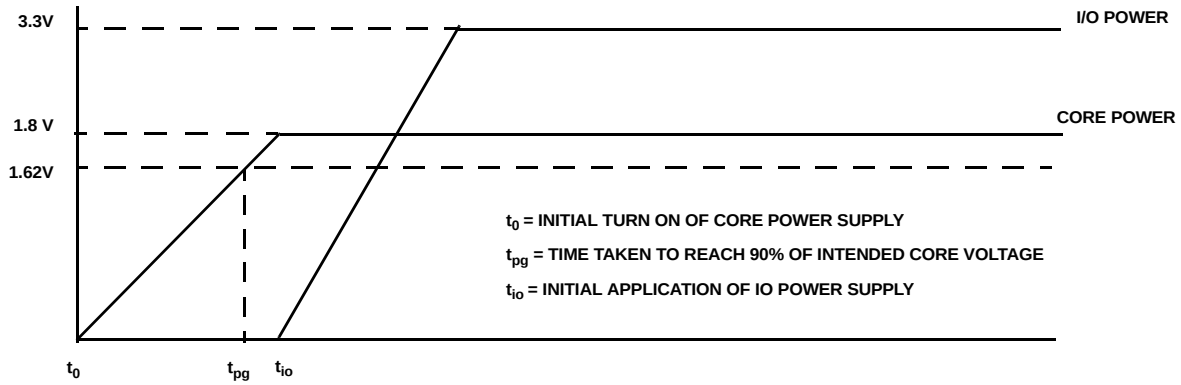


Figure 5: Power Sequencing

13 Outline Diagrams

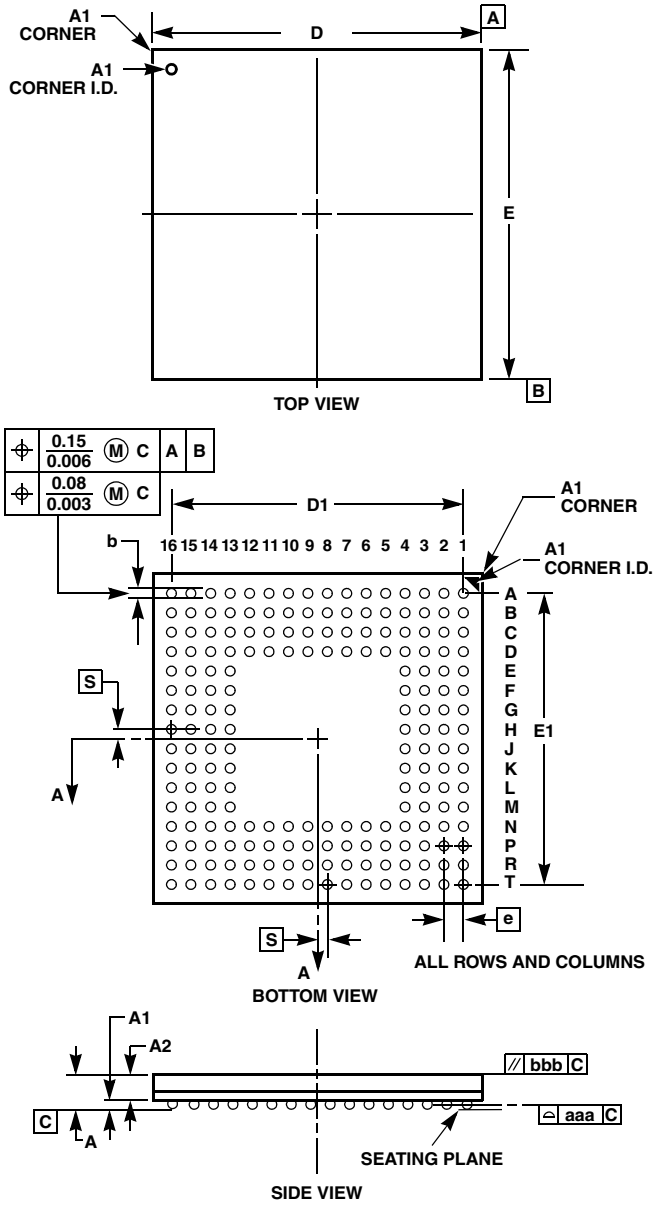


Figure 6: Plastic Ball Grid Array Packages (BGA)

Table 5: V192.14x14B 192 Ball Plastic Ball Grid Array Package

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	-	0.047	-	1.20	-
A1	0.010	0.014	0.25	0.35	-
A2	0.026	0.035	0.67	0.90	-
b	0.014	0.018	0.35	0.45	7
D/E	0.547	0.555	13.90	14.10	-
D1/E1	0.468	0.476	11.90	12.10	-
N	192		192		-
e	0.032 BSC		0.80 BSC		-
MD/ME	16 x 16		16 x 16		3
bbb	0.004		0.10		-
aaa	0.005		0.12		-

NOTES for Figure 6 and Table 5:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. “MD” and “ME” are the maximum ball matrix size for the “D” and “E” dimensions, respectively.
4. “N” is the maximum number of balls for the specific array size.
5. Primary datum C and seating plane are defined by the spherical crowns of the contact balls.
6. Dimension “A” includes standoff height “A1”, package body thickness and lid or cap height “A2”.
7. Dimension “b” is measured at the maximum ball diameter, parallel to the primary datum C.
8. Pin “A1” is marked on the top and bottom sides adjacent to A1.
9. “S” is measured with respect to datum’s A and B and defines the position of the solder balls nearest to package centerlines. When there is an even number of balls in the outer row the value is “S” = e/2.

14 Order Information

Table 6: Ordering Information

Part Number	Package	Package Drawing #	Temp. Range (°C)	Pack Method	Minimum Orderable Quantities
GW3887AIK	192 Pin BGA	V192.14x14B	-40 to 85	Tray	90
GW3887AIK-TK	192 Pin BGA			Tape and Reel	1000
GW3887AIKZ-TK[a]	Lead Free192 Pin BGA			Tape and Reel	1000

a. Lead Free products employ special lead free material sets; molding compounds / die attach materials and 100% lead free termination finishes, which are compatible with both SnPb and lead free soldering operations. Lead Free products are MSL classified at lead free peak reflow temperatures that meet or exceed the lead free requirements of IPC/JEDEC J Std-020B.

For additional information, contact Conexant Systems, Inc. (together with its subsidiaries, “Conexant”) at **1-888-855-4562** (toll-free within the U.S. and Canada) or **1-732-345-7500**, or visit the Conexant internet site at www.conexant.com.